LAB REPORT

JVL2384 (PRANAV KUMAR RAI)

PROCEDURE

First of all, made schematic and layout of INVERTER

Then of

NAND2

AND2

NAND3

SR LATCH

JK FF

MOD\_5\_SYNCHRONOUS\_UP\_COUNTER

Simulated each circuit

Cleared all DRC error of each circuit

Cleared LVS error of each circuit

I have attached the Schematic, layout, Simulation, DRC, LVS, PEX reports.