LAB REPORT

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AIM

To Design MOD5 Synchronous Up Counter using JK Flipflop

PROCEDURE

First of all, made schematic and layout of INVERTER

Then of

NAND2

AND2

NAND3

SR LATCH

JK FF

MOD\_5\_SYNCHRONOUS\_UP\_COUNTER

Simulated each circuit

Cleared all DRC error of each circuit

Cleared LVS error of each circuit

I have attached the Schematic, layout, Simulation, DRC, LVS, PEX reports.

RESULTS

Frequency of operation 250Mhz

Counter input CLK

Counter Output Q2 Q1 Q0

Different states of counter

000 001 010 011 100 000 001 so on